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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,304	11/14/2003	Chao-Cheng Chen	TS02-210	2110

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EXAMINER	
ESTRADA, MICHELLE	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/714,304	CHEN ET AL.	
	Examiner	Art Unit	
	Michelle Estrada	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-50* is/are allowed.

6)☒ Claim(s) *1,4-8,10-14,16 and 18,19,21 and 22* is/are rejected.

7)☒ Claim(s) *2,3,9,15,17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 4-8, 10-14, 16 and 18, 19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito (US2004/0166669) in view of Kawai et al. (US 2003/0054629).

With respect to claim 1, Saito discloses providing a structure having an overlying exposed conductive layer (1) formed there over; forming a dielectric layer (2) over the conductive layer Page 1, Paragraph [0027]; etching the dielectric layer using a via opening process to form an initial via (3) exposing a

portion of the conductive layer (See Fig. 1B and Page 2, Paragraph [0028]); forming a protective film portion (4) over at least the exposed portion of the conductive layer (Page 2, Paragraph [0029]); patterning the dielectric layer (2) to reduce the initial via to a reduced via and to form a trench opening (6) substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening (See Figs. 1E, 1F and Page 2, Paragraphs [0030], [0031] and [0032]).

Saito does not disclose forming an anti-reflective coating layer over the dielectric layer and etching the anti-reflective layer to form an initial via; and then patterning the anti-reflective layer to reduce the initial via.

Kawai et al. disclose providing a structure having a conductive layer (2) (Page 3, Paragraph [0047]); forming a dielectric layer (3) over the conductive layer (Page 3, Paragraph [0048]); forming an anti-reflective coating layer (4) over the dielectric layer (Page 3, Paragraph [0049]); etching the anti-reflective layer (4) and the dielectric layer using a via opening process to form an initial via (6) (See Fig. 1A and Page 3, Paragraph [0050]); forming a protective film portion (17) (See Fig. 1B and Page 3, Paragraph [0053]); patterning the anti-reflective locating layer and the dielectric layer (3) to reduce the initial via to a reduced via and to form a trench opening (10) substantially centered over the reduced via; the trench opening and the reduced via comprising the dual damascene opening (See Fig. 1C and Page 3, Paragraph [0054]).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Saito and Kawai et al. to enable the anti-reflective

coating layer formation step of Kawai et al. to be performed in the process of Saito because it will improve the dimension accuracy of the initial via (6) (Page 3, Paragraph [0051] of Kawai et al.

Re claim 4, Kawai et al. disclose wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of less than about 3.0.

Re claim 5, Kawai et al. disclose wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.0 to less than about 3.0.

Re claim 6, Kawai et al. disclose wherein the dielectric layer is a porous low-k dielectric layer having a dielectric constant of from about 1.5 to 2.8.

Re claim 12, Kawai et al. disclose including the step of forming an etch stop/liner layer (16) over the exposed conductive layer.

Re claim 13, Kawai et al. disclose disclose including the step of forming an etch stop/liner layer (16) over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 200 to 1500 Å, which overlaps the recited thickness of claim 13 (50 to 2000 Å) and being comprised of the elements Si and C such as SiC.

Re claim 14, Kawai et al. disclose disclose including the step of forming an etch stop/liner layer (16) over the exposed conductive layer; the etch stop/liner layer having a thickness of from about 200 to 1500 Å, which overlaps the recited thickness of claim 13 (100 to 1000 Å) and being comprised of the elements Si and C such as SiC.

Re claim 16, Saito discloses wherein a via plug is formed within the initial via before formation of the trench opening (See Fig. 1B).

Re claim 18, Saito discloses wherein the formation of trench opening utilizes a patterned photoresist masking layer (5) as a mask.

Re claim 19, Saito discloses wherein the formation of trench opening utilizes a patterned photoresist masking layer (5) as a mask.

Re claims 7, 8, 10, 11, 21 and 22, One of ordinary skill in the art would have been led to the recited thicknesses, temperature, pressure time and plasma power through routine experimentation to achieve a desired rate of annealing, device dimension, device associated characteristics and device density on the finished wafer. See MPEP 2144.05. In addition, the selection of thicknesses, temperature, pressure time and plasma power, it's obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species of result effective variables. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996)(claimed ranges or a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill or art) and In

re Aller, 105 USPQ 233 (CCPA 1995) (selection of optimum ranges within prior art general conditions is obvious).

Note that the specification contains no disclosure of either the critical nature of the claimed thicknesses, temperature, pressure time and plasma power or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen thicknesses, temperature, pressure time and plasma power or upon another variable recited in a claim, the Applicant must show that the chosen thicknesses, temperature, pressure time and plasma power are critical. *In re Woodruf*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Allowable Subject Matter

Claims 2, 3, 9, 15, 17 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 23-50 are allowed.

The following is an examiner's statement of reasons for allowance: Re claim 23, there is no disclosure in the prior art of forming a protective film portion over at least the exposed portion of the conductive layer; the protective film portion being comprised of the elements C, H and O such as C_2H_4 or C_2H_6. Re claim 43, there is no disclosure in the prior art of etching the anti-reflective layer and the dielectric layer using a via opening process to form an initial via exposing a portion of the etch stop/liner layer; and removing the exposed portion of the

etch stop/liner layer using a liner removal process to expose a portion of the underlying conductive layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is 571-272-1858. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-0224 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michelle Estrada
Examiner
Art Unit 2823

ME
April 18, 2005